Dynamic Approaches to Mixed – Signal Design

Angel Nikolaev Popov

Abstract - **The present paper is devoted to three approaches and corresponding design techniques aimed at improving some mixed – signal circuits in terms of noise immunity (NI), power consumption and accuracy. The first approach, named Dynamic Hysteresis (DH) is based on the proposed Schmitt trigger which features only one threshold and time controllable hysteresis. The second one use Dynamic Current Control (current mode switching) and reduces to a half the power needed for topology symmetrical circuits e.g. emitter – coupled multivibrators (ECM) and voltage/current controlled oscillators (VCO/CCO). The third approach is a sort of Dynamic Element Matching(DEM) achieves a precise divide-by-two by means of switched capacitors (SC) and additional processing.**

Keywords – **Mixed-signal circuits, noise immunity, dynamic hysteresis, current mode, SC circuits.**

I. INTRODUCTION

"It is important to design circuits with both a circuits and a systems perspective in mind"
Jan Rabaey [1].

This lecture has three reasons to be presented. The first one is formal – I was invited to. The second, however, and major reason is the need of mixed-signal circuits for the modern large Systems-on-Chip (SoC) [5]. SoC is a concept that integrates pre-designed, reusable components, so called Intellectual Property (IP) cores. At first glance, though there are some hidden hurdles, the pure digital SoC design seems easy and – as a joke – could be named "Mouse Aided Design". But analog, RF and mixed-signal cores still are not easy portable and could cause a wide range of problems in terms of compatibility, power consumption, noise emissions and immunity, area etc. The general today's tendency is to use digital CMOS process for all IC products, including – certainly – mixed-signal circuits. But this process is optimized mainly for digital designs trading-off between speed, power and area. Razavi [6] points out that analog and mixed-signal circuits entail a multidimensional design space. The author also offer an octagon where every two parameters trade with each other. Moreover the Deep Submicron Technology (DST) deteriorates some important for analog design transistor characteristics. Besides the search for new approaches, some ones can be borrowed from the digital design and applied in a more and more digitally assisted mixed signal design.

Last but not least, the third reason is that from author's point of view this presentation is retrospective, in other words it is a sentimental journey to past Sozopol's conferences, where most of these ideas and designs have been reported.

The purpose of this work is to consider a few insights into the design of mixed-signal system components as well as to propose and discuss some ideas concerning their behavior and schematics. Because the real design – more or less – is a parallel flow of two streams: "top-down"(started from system level) and "bottom-up" (started from transistor level), which finally meet each other at the point "middle-out". The main parameters under consideration and the interaction between them are presented in the hexagon of Fig.1, according to the upper mentioned idea of Razavi [6].

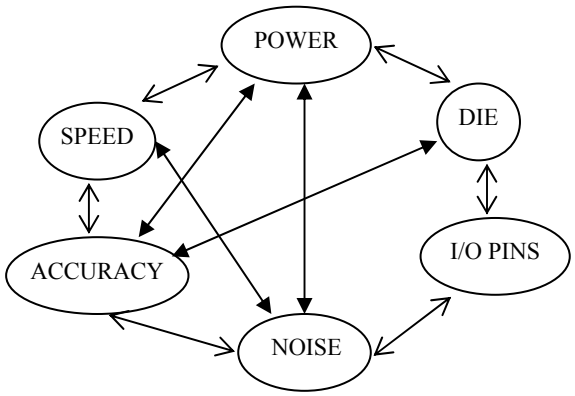

Fig.1. Parameters and design trade-off

As for the correspondence between the title and the content of this presentation, it may well be true the field of mixed-signal design is rather problem-driven than suggested by some approaches. Perhaps the approaches are engendered by new devised circuits and being generalized by every following successful design. Moreover usually it turns out impossible to explain a sophisticated circuit by a single approach. A common feature of all three approaches to be reported is they are dynamic, i.e. they are mainly connected with the time.

The contents is structured as follows. Section II is dedicated to the proposed dynamic hysteresis, related circuits and application to analog-to-digital conversion. In Section III are synthesized high-speed voltage- and current controlled oscillators featuring reduced voltage supply and power consumption. Section IV is devoted to an original algorithm for precise divide-by-two, switched-capacitor implementation of the algorithm and the application to digital-to-analog converter design. Concluding remarks are given in Section V

So, let's start discussing one by one three approaches to mixed signal circuit design having in mind Einstein's warning:

"Everything should be made as simple as possible – but no simpler"

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II. NOISE IMMUNITY – DYNAMIC HYSTERESIS

"The best way to have a good idea is to have a lot of ideas", Linus Pauling

The Schmitt trigger was invented in 1934 by Otto H. Schmitt (1913-1998) while he was still a graduate student, later described in his doctoral dissertation (1937) as a "thermionic trigger" [7]. It was a direct result of Schmitt's study of the neural impulse propagation in mollusca's nerves. Schmitt is known for his scientific contributions to biophysics and for establishing the field of biomedical engineering. He also invented the cathode follower, the differential amplifier, and the chopper-stabilized amplifier.

The Schmitt Trigger, as defined by its inventor: A bistable positive feedback circuit, realizable with vacuum tubes or even fluidic components, but now usually solid-state electronics, which features a selected or adjustable hysteresis band separating initiation of "on" and "off" or "1" and "0" states [7].

The "secret" behind the Schmitt trigger (ST) concept, its driving force, is the use of positive feedback (PF). It causes fast transition time at the output and two different input thresholds (hysteresis). Thanks to these features ST is used mostly to turn noisy or slowly varied input signals into clean digital output signals. Hence ST is very convenient for comparator circuits, except to the fact that a comparator needs only one switching threshold for positive- and negative-going input signal. Is it possible keeping the inherent ST's speed and noise – immunity to create new schematics with only one input threshold? This is the problem. How to solve it?

A. Getting the idea [8]

Voltage-transfer characteristic of a noninverting Schmitt trigger and its schematic symbol are shown in Fig. 2. The next Fig. 3 depicts a ST circuit, input/output signals and the variations of the threshold between both levels – higher $VT+$ and lower $VT–$. It worth to note between two switchings the threshold stays stable. It is known that for a system with feedback (Fig.4a) the gain K_F equals

$$K_F = \frac{K_0}{1 - \beta K_0}\ , \tag{1}$$

where K_0 is the gain without feedback and β is voltage-transfer coefficient of the PF circuit itself. The necessary and sufficient condition for existing of trigger effect is

$$\beta K_0 > 1. \tag{2}$$

The value of the product βK_0 determines also the width of the hysteresis

$$\Delta V_H = V_{T+} - V_{T-} \tag{3}$$

For our purpose the threshold level must behave as is shown in Fig. 4b. This should be feasible if every switching generates after some delay t_D a signal to stop PF operation – by neutralizing or breaking it off – and restore initial value V_{ref} of the circuit threshold (Fig. 4c). So during a period of time t_D the input reference voltage changes to be in the opposite direction of the input signal change. This time-domain phenomenon is called by the author "**Dynamic Hysteresis**"(DH) [8,9,12]. If the interval t_D is controllable then the time domain insensibility should be adapted so that the noise added to the input signal to be rejected.

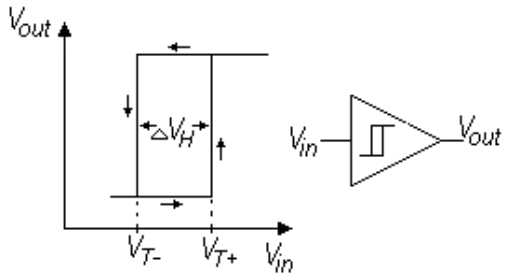


Fig. 2. Noninverting Schmitt trigger

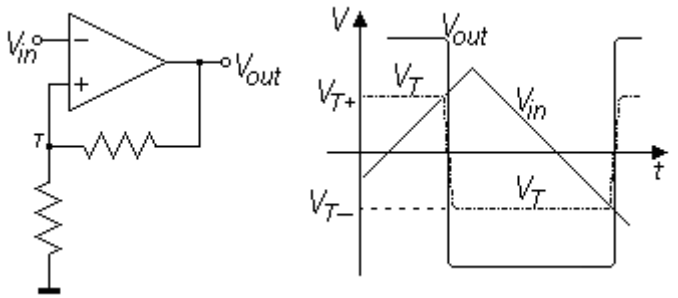
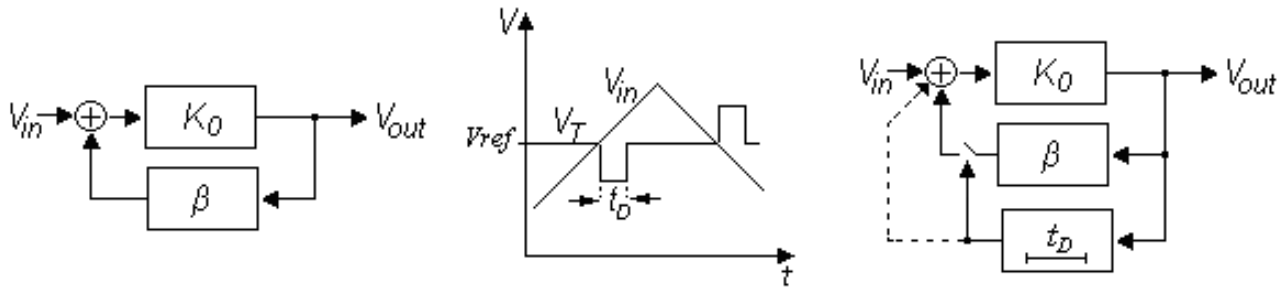


Fig. 3. Noninverting Schmitt trigger and its signals



a) b) c)

Fig. 4. Synthesis of a Schmitt trigger with dynamic hysteresis

B. Circuit based on two OpAmps

First ST with DH [8] has been created by using two operational amplifiers (Fig. 5).

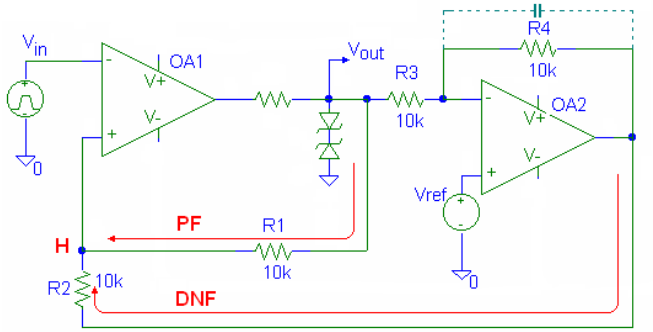


Fig. 5. Circuit based on two OpAmps

The first one along with the resistors R_1 and R_2 is a conventional ST. The second amplifier provides a delayed negative feedback (DNF), precisely equal, but opposite to the PF of the ST. The comprehensive analysis made in [8] give in closed form some basic results, that are in good agreement with the experiments and simulations. For instance if

$$R_1R_4 = R_2R_3, \tag{4}$$

then the voltage $V_H = V_{ref}$ with the exception of the transients during the DH. Hence the input threshold coincides with the value of Vref in wide range. On the other hand the time duration of the DH can be changed by the delay of the second stage, e.g. by a Miller capacitor (with a broken line in Fig. 5).

C. CMOS circuits

Circuit design technique is based on a CMOS Schmitt trigger (Fig. 6) proposed in [21]. The developed topology shown in Fig. 7 is entirely symmetrical. A chain of odd number inverters represents the DNF. PF and DNF signals interact through transistor cascades M_3, M_4 or M_5,M_6[11].

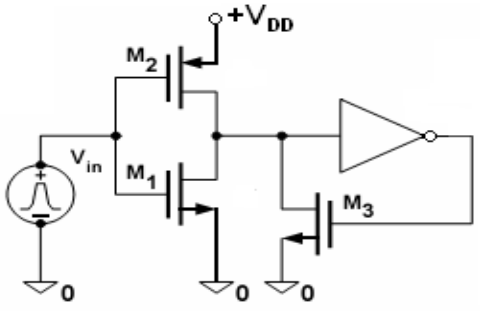


Fig.6. CMOS Schmitt trigger proposed in [21]

Let us suppose the input voltage level is below the threshold of the input inverter (M_1,M_2). The output voltage (inverter M_7,M_8) is low and transistor M_4 is off. At the same time the NF output (M_{13},M_{14}) is high, transistor M_3 is on, allowing operation of the PF. When a raising signal reaches the input inverter threshold, the PF (inverter M_6,M_7 and transistor M_4) begins switching. As a result the output signal of M_1,M_2 decreases, making the circuit insensible to fast changes, respectively noises, of the input signal. After arriving of the delayed NF signal, transistor M_3 switches from on to off, interrupts the PF loop and restores the initial threshold. The opposite switching process caused by a decreasing input signal is the same, but the upper cascade M_5,M_6 is used for interaction of both feedbacks.

The amplitude of the noise to be suppressed depends of the area ratio of M_3M_4 to M_1, respectively M_5M_6 to M_2 (Fig. 7). Simulated waveforms in Fig. 8 and Fig. 9 show the behavior of a comparator with noise immunity of 1V when the amplitude of the noise is less or bigger than 1V.

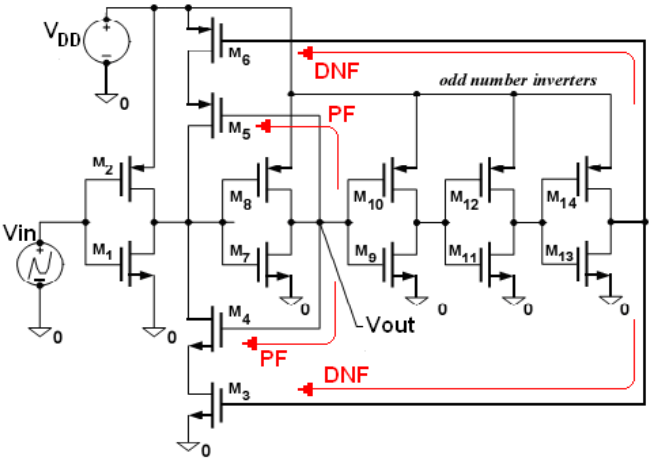


Fig.7. CMOS Schmitt trigger

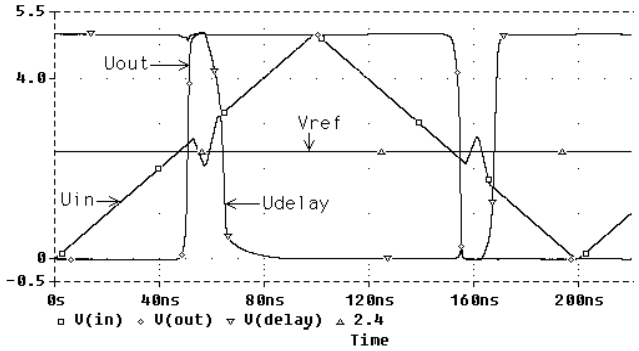


Fig. 8. Simulated waveforms showing the behavior of a comparator with noise immunity of 1V when the amplitude of the noise is less than 1V.

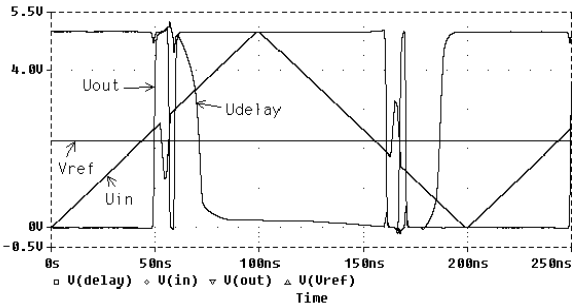


Fig. 9. Simulated waveforms Simulated waveforms showing the behavior of a comparator with noise immunity of 1V when the amplitude of the noise is bigger than 1V

The next Fig. 10 shows the experimental result demonstrating the expected one threshold behavior of the circuit in Fig. 6. In [23] is proposed bulk-driven method for control of the gate delay. It is verified by simulating CMOS ring oscillator and is very convenient for changing DH time duration [13,14].

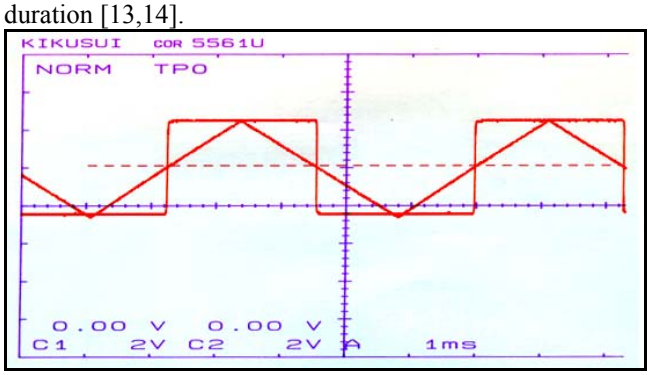
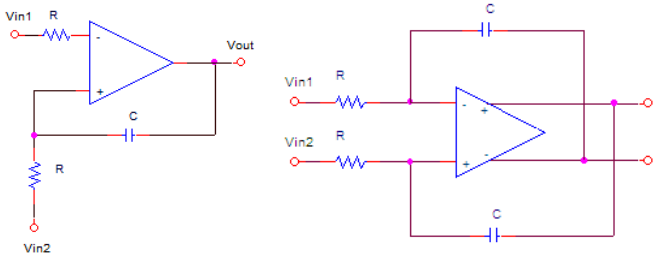


Fig. 10. Experimental result demonstrating the expected one threshold behavior of the circuit in Fig. 6.

D .BJT circuit

The generalized structure of DH circuit (Fig. 4c) suggests an opportunity to simplify the design, inserting a capacitor into the PF loop (Fig. 11a). The charge/discharge of the capacitor C through a resistor R determines the duration of PF operation, i.e. the time-domain insensibility to input noises. Consequently, there is no need of DNF. A symmetrical version of this principle is shown in Fig. 11b. The detailed schematic of the proposed comparator and its operation are depicted in Fig. 12 and Fig. 13, respectively [10].



a) b)

Fig.11. ST circuit with a capacitor inserted in the PF loop

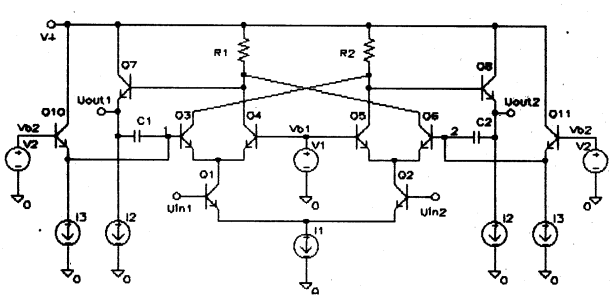


Fig. 12. BJT comparator

The circuit is based on the use of bipolar junction transistors (BJTs). The symmetrical stacked topology relies on emitter-coupled design style. It consists of a differential stage which controls the emitter currents of two Schmitt triggers. They are additionally cross-coupled in order to reinforce the avalanche-like switching process and to lock out each other against noises. The bias voltages V_{B1} and V_{B2} are chosen so that in a steady-state the transistors Q_3 and Q_6 to be kept slightly off whereas Q_4 and Q_5 are on.

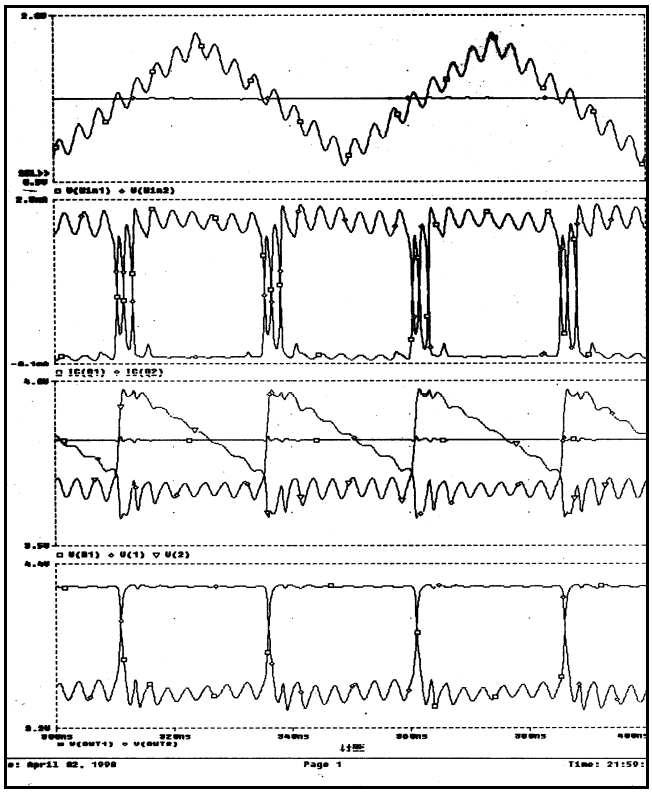


Fig. 13. Waveforms demonstrating the operation of the BJT comparator

Thanks to this and to the capacitors, any races or oscillations are impossible, but at the expense of rejecting very slowly changing analog input signals.

Let us suppose (Fig. 13) a raising triangular "noisy" input signal V_{in1} crosses the reference voltage V_{in2}. The PF boosts rapidly V_{out1} to high and V_{out2} to low level. The positive pulse at the output1 switches completely the common current I_1 through Q_3, making the base of Q_3 (point 1) rather more positive than the bases of Q_4, Q_5 and Q_6. This is the cause of short-time circuit insusceptibility to noises. It is clearly visible that relatively large input signal fluctuations, changing dramatically the currents through Q_1 and Q_2, do not influence the state of the outputs. The base voltage V_1 of Q_3 decreases slowly because of discharging the capacitor by the base current of Q_3 and the current source I_3. This process determines the time interval of noise immunity t_{NI}:

$$t_{NI} = \frac{CV_M}{I_3}, \tag{5}$$

where $V_M = R_C I_1$ is the output voltage swing. Therefore t_{NI} could be controlled by varying I_3.

E. Aapplication – Analog-to-Digital Converter Design

The bursting development of mixed-signal system-on-chip applications leads to a growing need of more sophisticated in terms of speed, area, noise immunity, etc., circuit designs[5]. This is particularly important in ADC design, which is often the bottleneck in the design of SOC solutions. The flash architectures constructed of latched comparators are preferred for their speed and inherent monotonicity, but suffer from large area and power dissipation. In addition, the latched comparators cause substantial noises on the input signal (kickback noise [6]) and on the supply voltage lines. Here the design is presented of a high noise immunity resistorless ADC.

In an earlier work [16] a resistorless asynchronous parallel ADC (Fig. 14) was proposed. It uses simple CMOS inverters (Fig. 15) instead of comparators. The proposed design has the advantage of smaller size because of the lacking resistor ladder and less noise due to the signal controlled switching of the comparators.

In [22] a similar architecture is proposed. It consists of two cascaded threshold inverter comparators and a gain boosting stage. The comparator threshold voltages VTHI are obtained by simulation. In standard 0.25µ CMOS technology the authors obtain an operation speed of 1 GSPS.

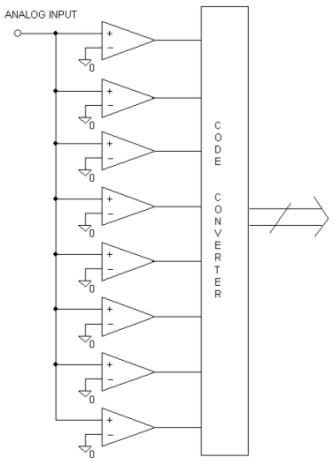


Fig. 14. Parallel resistorless ADC

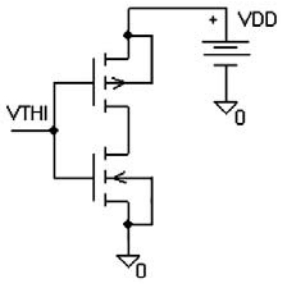


Fig. 15. CMOS inverter used as comparator

The present work applies the method for standard 0.18µ and 0.07µ CMOS technology. An investigation of the static and dynamic behavior of the ADC is performed to explore its maximal resolution and frequency of operation without missing code. The boosting stage used in [22] to increase the comparator gain was replaced by a Schmitt trigger with time controllable noise immunity developed by the authors [16,18,19,20].

E1. Threshold Voltage Determination

The threshold voltage V_{THI} of the inverter depends of the transistor area ratio of the *N*-channel and *P*-channel MOS transistors. The analytical solution for V_{THI} given in [4] neglects the short channel effects and is not applicable for 0.18µ technology. The dependence of the threshold voltage of transistor area ratio is obtained by simulation. The values of the comparator parameters are as follows: $V_{DD} = 2.5$V, $k = 0.45 \div 20$, $W_N/L_N = \text{const}$. The resulting characteristic is given in Fig. 16.

The non-shaded area of the plot corresponds to the chosen range of 0.95V for V_{THI}. A *PSpice* macro was used to construct the step function, from which the values of transistor area ratio k for a chosen level of quantization were determined. The procedure can be easily adapted to different transistor models, input voltage full-scale range and ADC resolution.

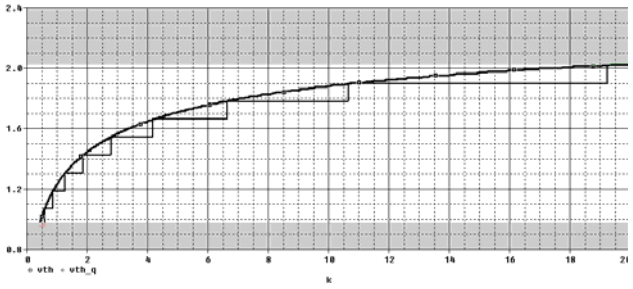


Fig. 16. Inverter threshold voltage V_{THI} as a function of transistor area ratio k

E2. ADC Investigation

The method of area size determination was applied for a level7 0.18µ CMOS technology with minimum square size of 0.44µ. As an example a 3-bit ADC was simulated and eight values of k were determined (Table 1).

TABLE I TRANSISTOR AREA RATIO

V_{THI}, V	k	P□/N□
1.06875	0.644	0.18 / 0.28
1.1875	0.911	0.18 / 0.19
1.30625	1.311	0.24 / 0.18
1.425	1.889	0.34 / 0.18
1.54375	2.711	0.49 / 0.18
1.6625	4.111	0.74 / 0.18
1.78125	6.155	1.11 / 0.18
1.9	9.822	1.77 / 0.18

The area of the top-most comparator does not follow its resolution by an exponential law, but depends rather on the input voltage full-scale range. For instance, for $V_{FSR} = 950$ mV, $k_{max} \sim 9.882$, regardless of the chosen ADC resolution.

E3. Transfer characteristics

The values of the threshold voltages V_{THI} were recorded at the point of the transfer characteristic where the input voltage of the inverter equals its output voltage. A grid of equally spaced characteristics was obtained. Afterwards, as in [2], a stage of two cascaded inverters was used to increase the gain and to sharpen the transfer characteristic (Fig. 17). For the second stage the transistor area ratio was chosen k=8/4 to obtain optimal values for $V_{TH2nd} \sim ½\ V_{DD}$ and approximately equal rising and falling edge delays.

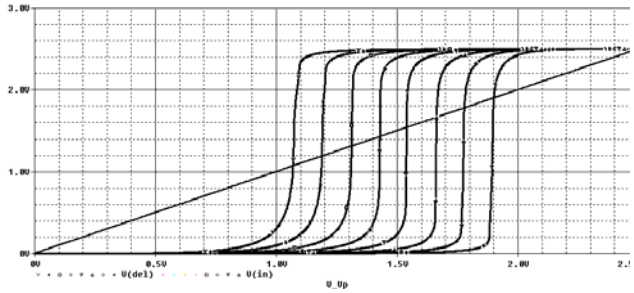


Fig. 17. Threshold voltage grid for a 3-bit ADC with two cascaded inverters

The second inverter was then replaced by a boosting stage consisting of a Schmitt trigger with time-controllable noise immunity and a single threshold [3,5,6]. The resulting transfer characteristics are shown in Fig. 18.

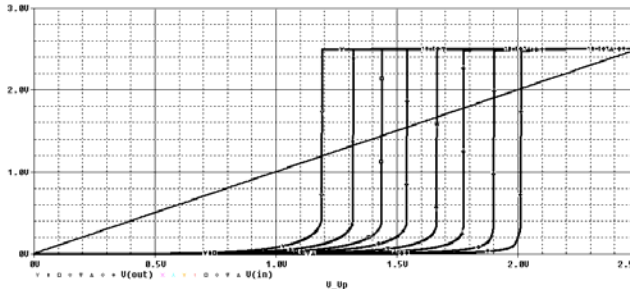


Fig. 18. Threshold voltage grid for a 3-bit ADC with an inverter and a dynamic hysteresis Schmitt trigger

E5. Dynamic behavior

The time-domain analysis shows that the proposed ADC may operate at speeds up to approximately 1GHz without missing codes. For an input signal with frequencies higher than 0.1GHz the switching of the comparators for the rising and the falling edge occurs at different threshold voltages.

The inverter delays for each bit of the ADC have been investigated (Fig. 19). It can be seen that the circuit with two cascaded inverters shows a larger delay than the one with a Schmitt trigger. The ADC delays in thermometer code as a function of *k* for an inverter booster and .a Schmitt trigger booster are presented in Fig. 20.

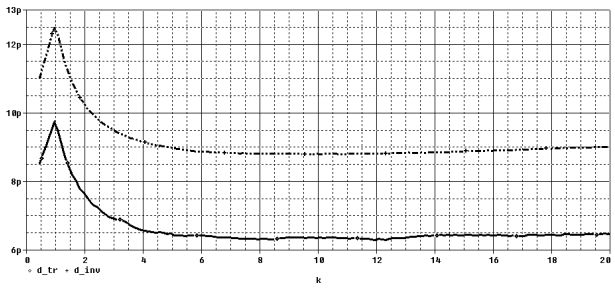


Fig. 19. ADC delays in thermometer code as a function of *k* for an inverter booster (dashed) and .a Schmitt trigger booster (solid)

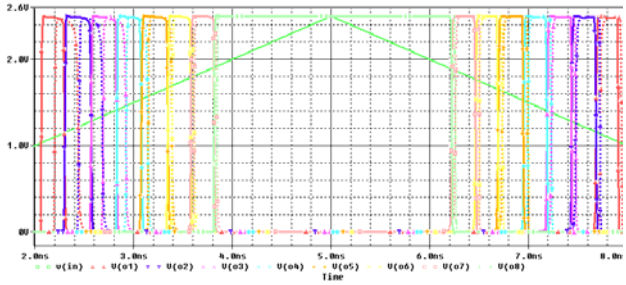


Fig. 20. ADC delays in thermometer code as a function of *k* for an inverter booster (dashed) and .a Schmitt trigger booster (solid)

Concluding Section II it worth to underline that the dynamic hysteresis approach design combines in a single circuit three features: high speed, noise immunity and precision and offers new areas for many applications.

III. Power Consumption – Current Mode Switching

"A good scientist is a person with original ideas. A good engineer is a person who makes a design that works as few original ideas as possible" .Dyson [3]

Emitter-Coupled Multivibrator (ECM) has focused for many years the efforts of the Phase-Locked-Loop (PLL) designers. Since, if a SoC could be viewed as a person and the on-chip-processors is regarded as its brain, then the PLLs is the heart. The main part of a PLL is voltage- or current-controlled oscillator (VCO or CCO).

The assets of the classic ECM have been perfectly summarized by B.Gilbert [24]. This symmetrical astable relaxation oscillator is simple, needs a single capacitor for timing and is ideally suited for monolithic fabrication. Its configuration results in large charging voltages being available across the capacitor even at low supply voltages (1-1.2V) for improved stability and jitter. The tight coupling within the regenerative loop minimizes nonlinearity caused by transit-time and switching delays [].

Over last two decades numerous ECM circuits have been developed [25,26,27,29]. Very sophisticated, they feature high performance parameters concerning precision, stability, controllability etc. but at the expense of power consumption and supply voltage as high as 4 – 5 V. Are the possibilities of the "brave old ECM" exhausted, or it could meet today's requirements?

A. Classic Emitter-Coupled Multivibrator

This section is aimed at development of the simplest classic circuit (Fig. 21) to achieve low voltage supply, voltage/current frequency control, high speed and reduced power consumption. The technology used at that time (1994/95) was BiCMOS, but the same designs are also feasible in CMOS. The circuit topology is symmetrical (R_{c1}=R_{c2}=R_c, I_{c1}=Ic_2=I_o) and the operation is well known.

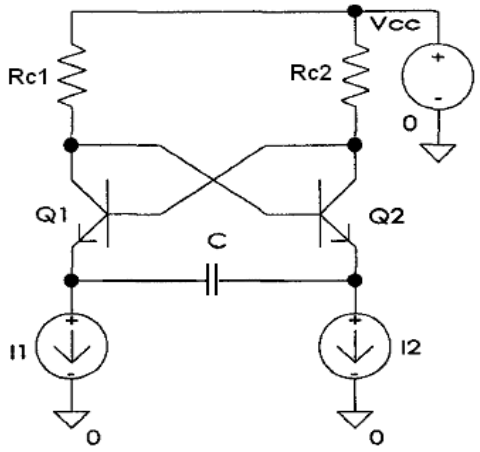


Fig. 21. Classic emitter-coupled multivibrator

There are two alternating quasistable states. During each of them one transistor is off, whereas the other one is on, but not saturated. To avoid transistor saturation the collector voltage swing, i.e. the amplitude V_M must be as low as 0.3-0.4V or $V_M \leq$ 0.3-0.4V. Let dwell on the state when Q_1 is on and Q_2 is off. The current source I_2 recharges the capacitor C till Q_2 begins to conduct. The duration of this process determines the half of oscillation period. At the instant when the gain of the positive feedback closed loop reaches unity, the circuit enters regenerative switching and changes quasistable state. During the next half-period Q_1 is off and Q_2 is on. The current source I_1 recharges the capacitor C till a new regenerative switching occurs. Hence the half-period and frequency are equal to

$$\frac{T}{2} = \frac{2V_M C}{I_0} \tag{6}$$

$$F = \frac{I_0}{4V_M C}, \tag{7}$$

where I_0 is the current flowing through the capacitor C, $V_M = 2\, I_0\, R_C$ is the amplitude and $2V_M$ is the voltage swing of the capacitor C.

A VCO as well as CCO feature a symmetrical topology and consist of three parts (sub-circuits): ECM cell, output buffers (usually – followers) and frequency control components [26]. All they form a circuit that require relatively high power consumption and supply voltages, incompatible with up-to-date SoC design. Their reducing is a must. But how? Moreover – without complicating the schematics….

B. Getting the idea

The symmetric topology and alternated quasistable states lead to the next idea: to use a single current and to switch it into the active half-part of the oscillator [30,31,33] . In Fig. 22 is shown the emitter coupled switching of the current I_o by the transistors Q_3 and Q_4. Theirs bases are controlled by a cross-coupling to the emitter follower outputs. Not only half power saving, but also precise time-domain symmetry is guaranteed. This approach of **Dynamic current control (current mode switching)** can be spread to the whole VCO/CCO schematics design.

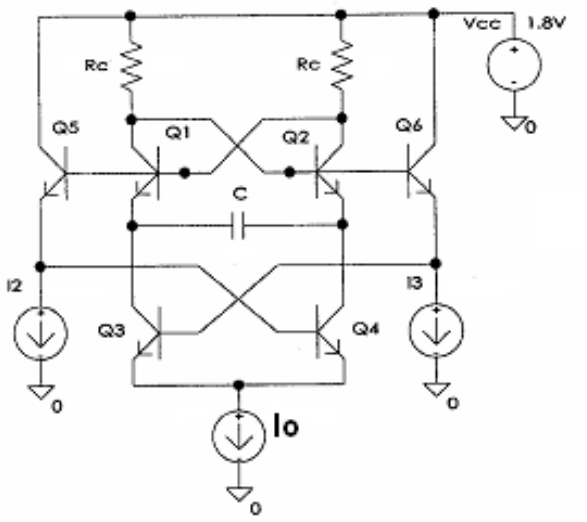


Fig. 22. Switching of the current I_o

C. Frequency control

The main obstacle to control the frequency by means of current *Io* is the correlation between V_M and *Io* (7).The most commonly used technique is based on diode clamping of collector voltage swings [26], so that V_M to be constant and dos not depend on *Io*. Here is proposed a circuit configuration in current switching style (Fig. 23). The goal is to sustain constant current through the transistor being on.

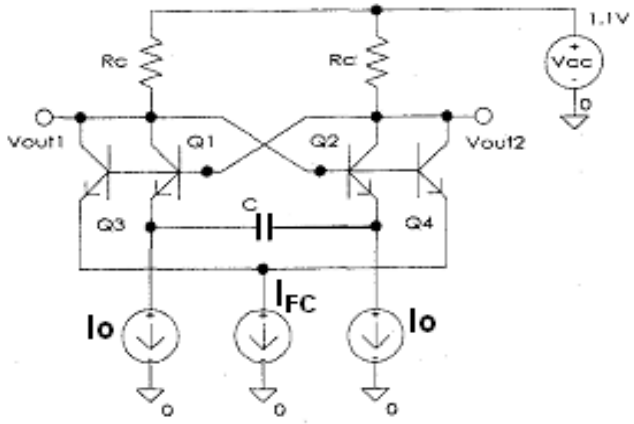


Fig. 23. Frequency control by switching current I_{FC}

The emitter-coupled pair Q_3-Q_4 switches an complementary current I_{FC} so that the sum of currents through Rc, respectively. amplitude V_M to be constant:

$$2I_o + I_{FC} = 2I_{omax} = \text{const}, \tag{8}$$

where I_{omax} determines the maximal working frequency.

D. VCO/CCO schematics

The CCO depicted in Fig. 24 [32,34] combines the techniques shown in Fig. 22 and Fig. 23.

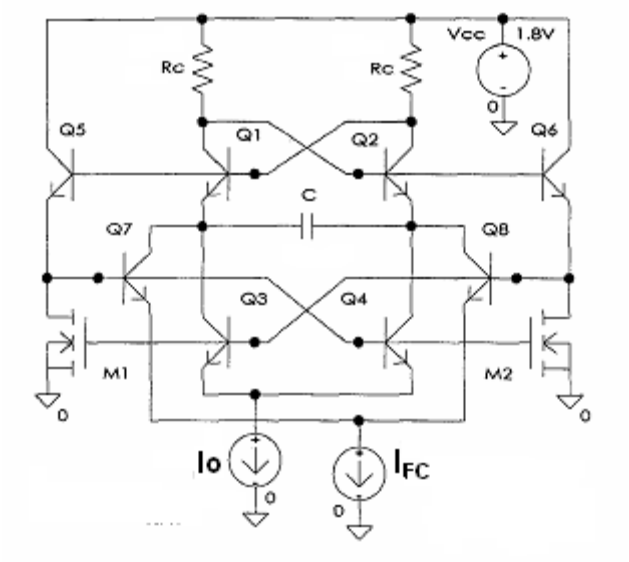


Fig. 24. CCO combining the techniques in Fig. 22 and Fig. 23

Dynamic current control is applied also to the output stages. The loads of the emitter followers are two cross-coupled NMOS transistors, representing an active-power technique, described in [28]. Each of the NMOS transistors discharge the output capacitance, whereas its counterpart is off. But due to the control of *Io* by the pair Q_3-Q_4, a shift of 0.7V is needed and a voltage supply increases up to 1.8V.

The most sophisticated CCO [35,36] shown in Fig. 25. keeps the lowest voltage supply of the classic ECM, but at the price of two currents I_o , instead of a single dynamically controlled one. Nevertheless this is the best CCO in terms of low voltage and low power. A voltage control, if needed, is shown in Fig. 26.

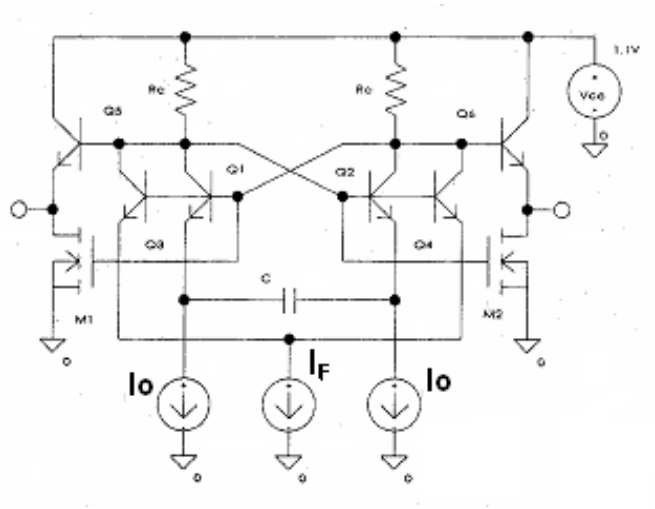


Fig. 25. CCO with the lowest voltage supply

In conclusion, the described in this section oscillators were analyzed by SPICE-simulation, using parameters of 0.8μm BiCMOS technology with bipolar NPN transistors with transient frequency 14 GHz. The circuits featured frequency over 2GHz, low voltage supply (1.2-1.8V) and power consumption (without output follower stages) within the range of 2 – 6 mW [ ].

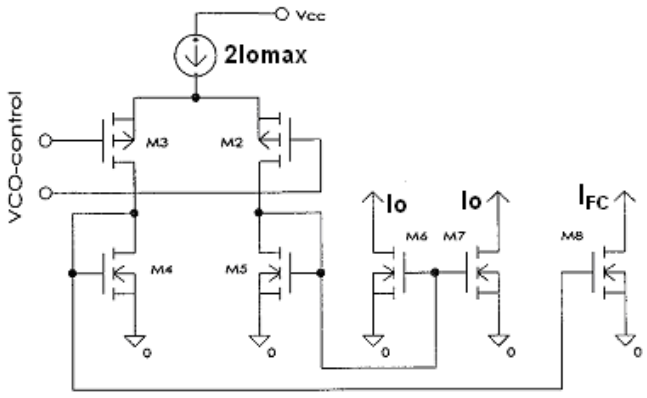


Fig. 26. Voltage control of the CCO in Fig. 25

IV. Accuracy – Precise Divide-by-Two

"A design is what the designer has when time and money run out" J. Poole[3]

Precise division by two is one of the most important signal processing operations in data conversion. Device matching (resistors in *R*-2*R* matrix, capacitors in charge redistribution converters, transistors in current steering DACs) is the ultimate limitation which forces analog designers to compensate this non-ideality by increasing the design size. This is not always possible since, unfortunately, the trend in analog design is to make more with less – i.e. – an accurate converter, which takes still less and less area in order to fit in a larger system and not increase the overall cost significantly.

With lower feature size technologies available nowadays it is possible to build a simple state machine or rather a phase sequence (even simpler) in order to dynamically match the devices which are to be used in the data converter. This approach makes the devices algorithmically almost equal.

This section presents an example circuit for an accurate divide by two operation, which can be used in the implementation of a low speed, high accuracy DAC.

A. Getting the idea

If a voltage is to be divided exactly by two, the designer needsperfectly matched devices. Provided that the capacitors differ from each other, additional signal processing is to be performed, such that the values of thecapacitors appear equal to a mean, whose exact value is unimportant. Statistically, we know that each capacitor can be represented as an average value, plus/minus a delta, common for both capacitors. If we charge the larger capacitor first and then redistribute the charge, the resulting value will be somehow bigger than the targeted middle of the initial voltage. Instead, if we decide to charge first the smaller capacitor, then the resulting value after redistribution will be somehow lowerthan the middle, but - with the same delta. It is exactly this property of charge

redistribution that is exploited here - perform charging in both directions (requires analog memory) and then average the result. After implementing this, we get a step closer to the target. Assuming that we perform these algorithmic steps an infinite number of times - we will end up with a perfectly divided voltage [42].

B. Two-capacitor DAC background

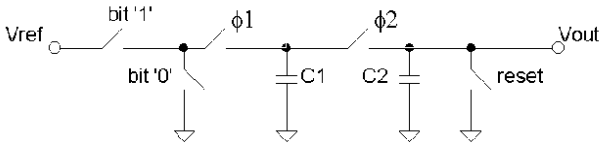


Fig. 27. Basic two-capacitor DAC schematics

One of the most area efficient digital – to –analog converters is the two-capacitor charge redistribution DAC [37] shown in Fig. 27. It consists only of two equal - valued capacitors and a few switches. The conversion is carried out as follows:

In the beginning the reset switch is closed. The digital code being converted is applied with its least significant bit first. The value of this bit drives switches bit'1' and bit'0'. Next Φ1 is activated and capacitor C_1 acquires V_{ref} or ground. During phase two Φ_2 is closed and the charge stored on C_1 is distributed among C_1 and C_2. If $C_1 = C_2$ exact division by two is accomplished. It can thus be shown that after N cycles the total output charge over C_2 will be:

$$Q_{c2} = C_2 V_{ref} \sum_{n=1}^{N} b_n 2^{n-N-1} \tag{9}$$

Several capacitor mismatch techniques have been described in the literature. Some implement a calibration cycle and storing digital correction terms in RAM [38]. Another method to improve linearity is to optimize the switching sequence for each input vector [39]. Since some kind of estimation is required, time and area are wasted for the completion of these correction cycles. Many other solutions [40] such as the splitting algorithm are also used [41], almost eliminating capacitor mismatch. However, this requires a ROM or an algorithmic unit to control the switching sequence, which compromises the DAC's main advantage – its small size.

The proposed method [42,43] does not remove capacitor mismatch error, but it does improve linearity a lot. What is important – it does not withal implement much additional elements and is as simple as the conversion algorithm itself.

C. Implementation of precise division by two

The algorithm consists of two consecutive cycles, each of which produces a voltage according to the selected charge pattern (i.e. which capacitor is chosen to be the charging one). Next, these two voltages are interchanged and applied to C_1 and C_2. The whole algorithm is described below.

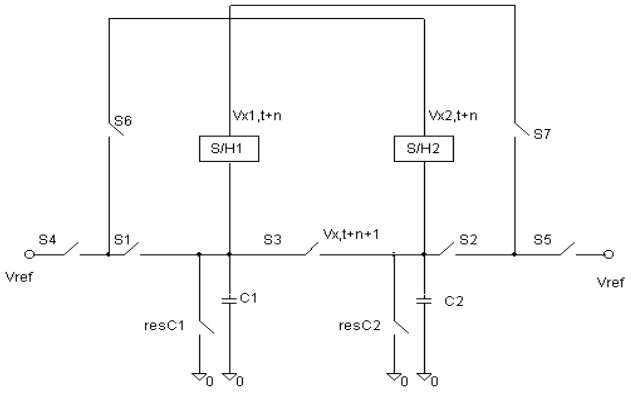


Fig. 28. Proposed schematics for precise division by two

Consider the schematic diagram in Fig. 28.

In the beginning of the conversion $Q_{C1}^{t} = 0$ and $Q_{C2}^{t} = 0$. Let the least significant bit is b_n. Switch S_4 is closed if b_n is '1' and switch res_{C1} is closed if this bit equals '0'. This charges C_1 with

$$Q_{C1}^{t+1} = C_1 V_{ref} b_n$$

Q_{C2}^{t+1} remains 0. After switch S_3 is closed the stored charges are summed, which results in

$$Q^{t+1} = C_1 V_{ref} b_n + 0 = V_{x1}{}^{t+1}(C_1 + C_2)$$

$$V_{x1}{}^{t+1} = V_{ref} b_n \frac{C_1}{C_1 + C_2}$$

This voltage is stored on S/H1. The operation is repeated but this time by charging C_2 to V_{ref} (or ground). By analogy, for $V_{x2}{}^{t+1}$ we obtain

$$V_{x2}^{t+1} = V_{ref} b_n \frac{C_2}{C_1 + C_2}$$

This voltage is stored on S/H2. Next, switches S6/S1 an S7/S2 are closed to enable C_1 to charge to V_{x2}^{t+1} and C_2 to charge to V_{x1}^{t+1}. This results in $Q_{C1}^{t+2} = C_1 V_{x2}^{t+1}$ and $Q_{C2}^{t+2} = C_2 V_{x1}^{t+1}$.

After the closure of S_3 the total charge will be

$$Q^{t+2} = C_1 V_{x2}{}^{t+1} + C_2 V_{x1}{}^{t+1} = V_x{}^{t+2}(C_1 + C_2)$$

$$V_x{}^{t+2} = \frac{C_1 V_{x2}{}^{t+1} + C_2 V_{x1}{}^{t+1}}{C_1 + C_2} =$$

$$= \frac{C_1 V_{ref} b_n \frac{C_2}{C_1 + C_2} + C_2 V_{ref} b_n \frac{C_1}{C_1 + C_2}}{C_1 + C_2} =$$

$$= V_{ref} b_n \frac{2C_1C_2}{(C_1+C_2)^2} \quad (10)$$

V_x^{t+2} is stored on both sample- holds. Next, bit b_{n-1} determines the position of S4 and resC1, thus charging C_1 to V_{ref} or discharging it to ground. C_2 still has its voltage equal to V_x^{t+2}. The charges on both capacitors is as follows $Q_{C1}^{t+3}=C_1V_{ref}b_{n-1}$ and $Q_{C2}^{t+3}=C_2V_x^{t+2}$. After the closure of S3 the total charge will be

$$Q^{t+3}= C_1V_{ref}b_{n-1} + C_2V_x^{t+2}=V_{x1}^{t+2}(C_1+C_2)$$

$$V_{x1}^{t+2} = \frac{C_1V_{ref}b_{n-1} + C_2V_x^{t+2}}{C_1+C_2}$$

This voltage is stored on S/H1. Now switches S6 and S1are activated and C_1 is charged to $C_1V_x^{t+2}$ (S/H2 still holds V_x^{t+2}). Switches S_5 (or resC2) and S_2 are also closed to give C_2 the charge of $C_2V_{ref}b_{n-1}$. Then, after redistribution, V_{x2}^{t+2} is equal to

$$V_{x2}^{t+2} = \frac{C_2V_{ref}b_{n-1} + C_1V_x^{t+2}}{C_1+C_2}$$

This voltage is stored on S/H2. Then switches S_6/$S_1$and S7/S2 are closed again. This produces the following charge on the capacitors

$Q_{C1}^{t+3}=C_1V_{x2}^{t+2}$ and $Q_{C2}^{t+3}=C_2V_{x1}^{t+2}$.

After the closure of S3 the total charge will be

$$Q^{t+3}= C_1V_{x2}^{t+2} + C_2V_{x1}^{t+2}=V_x^{t+3}(C_1+C_2)$$

$$= \frac{C_1\frac{C_2V_{ref}b_{n-1} + C_1V_x^{t+2}}{C_1+C_2} + C_2\frac{C_1V_{ref}b_{n-1} + C_2V_x^{t+2}}{C_1+C_2}}{C_1+C_2} =$$

$$V_x^{t+3} = \frac{C_1V_{x2}^{t+2} + C_2V_{x1}^{t+2}}{C_1+C_2} =$$

$$= V_{ref}b_{n-1}\frac{2C_1C_2}{C_1+C_2} + V_{ref}b_n\frac{(2C_1C_2)^2}{(C_1+C_2)^4}$$

$$= \frac{2C_1C_2(V_{ref}b_{n-1} + V_x^{t+2})}{(C_1+C_2)^2} \quad (11)$$

If we designate $\frac{2C_1C_2}{(C_1+C_2)^2}$ in (11) as w, substitute V_x^{t+2} from (10) and write the general form the following equation results

$$V_x^{t+k+1} = V_{ref}\sum_{k=0}^{N} b_{n-k}w^{k+1} \quad (12)$$

Let us compare the accuracy achieved by this method to the one without correction. If we represent C_1 and C_2 by means of a value C and an error capacitance of ΔC then we will obtain

$$\frac{C \pm \Delta C}{C \pm \Delta C + C \mp \Delta C} = \frac{C \pm \Delta C}{2C} = \frac{1}{2} \pm \frac{\Delta C}{2C}$$

The error is introduced by the second term. When swapping is applied this equation will look like

$$\frac{2(C \pm \Delta C)(C \mp \Delta C)}{4C^2} =$$

$$= \frac{C^2 \mp C\Delta C \pm C\Delta C - \Delta C^2}{2C^2} = \frac{1}{2} - \frac{\Delta C^2}{2C^2}$$

It is evident that an accuracy gain of $C/\Delta C$ is achieved.

For the sake of accuracy $\Delta C/C<1$LSB, i.e. $\Delta C/C<1/2^N$ (where N is the resolution of the DAC) in the conventional method. If we implement the algorithm described above this restriction is not so stringent.

$$\frac{\Delta C^2}{C^2} < \frac{1}{2^N} \Leftrightarrow \frac{\Delta C}{C} < \sqrt{\frac{1}{2^N}}$$

D. Results

Simulations have been performed to prove the feasibility of the proposed technique. Mismatch of 10% was chosen. We tested the worst case where both capacitors had the error capacitance summed with and subtracted from (for C_1 and C_2 respectively) the ideal capacitance C. The diagram shows the division by two of V_r=3V (Fig. 29). The erroneous voltages (seen at 1,5μs and 2,5μs) are placed almost symmetrically around the averaged one. The calculated output voltage is 1,485V. V_{x1} and V_{x2} are equal to 1,65V and 1,35V respectively. The selection of a large $\Delta C/C$ was made on purpose aiming more illustrative results.

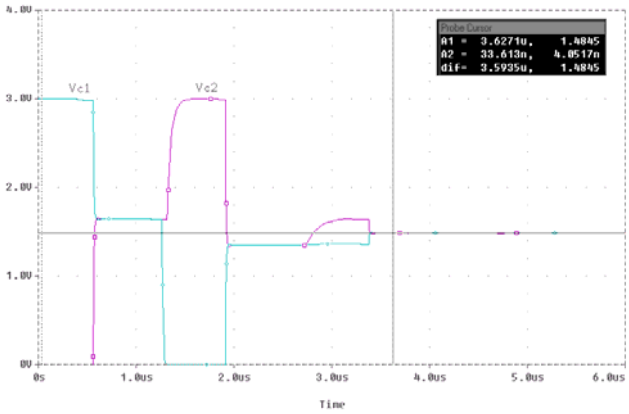


Fig. 29. SPICE simulation of the proposed algorithm

The method described in Section IV significantly reduces the effect of capacitor mismatch thus allowing the design of an accurate divide by two circuit, which can be used in the implementation of a two capacitor DAC. It should be mentioned that second order effects such as charge injection and clock feedthrough are not taken into account in this discussion. However, there are a lot of techniques described in the literature to mitigate the effect of these sources of error [6]. If the circuit is carefully deigned, the described algorithm can lead to a significant gain in overall area, still preserving the accuracy which would be otherwise achieved with much larger devices.

V. CONCLUSIONS

"There's Plenty of Room at the Bottom" R. Feynman[4]

Three dynamic approaches and corresponding techniques , proposed and investigated by the author, were described and discussed. The circuit design is aimed at application to up-to-date Systems-on-Chip. A look into the future should prove the sentence: The most "foolish" ideas at the highest level need respective support from the bottom level.

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